METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT

ABSTRACT OF THE DISCLOSURE

A method of fabricating an integrated circuit includes forming a barrier layer along lateral side walls and a bottom of a via aperture and providing a ternary copper alloy via material in the via aperture to form a via. The via aperture is configured to receive the ternary copper alloy via material and electrically connect a first conductive layer and a second conductive layer. The ternary copper alloy via material helps the via to have a lower resistance and an increased grain size with staffed grain boundaries.